REMARKS

Claims 1-13, 15, and 17-20 are pending in this application. Claims 1, 4, 7, 8, 13, 15, 17, and 19 are independent claims. Claims 2, 3, 5, 6, 9-12, 18, and 20 are dependent claims.

Claims 15 and 20 have been allowed. Claims 1-13 and 17-19 have been rejected. Amendments to claims 13 and 17 are presented herein. Claims 1-12, 18, and 19 have been cancelled in this response. Claims 21 and 22 are newly added in this response. Claims 13 and 17 have been amended to reinstate these claims as originally filed. Claims 21 and 22 have been added to reinstate originally filed claims 14 and 15, respectively. No new matter is being presented, and approval and entry are respectfully requested.

Objections to the Claims

In item 2 on page 2 of the Office Action, the Examiner objected to claims 7 and 19 because of various informalities. Claims 7 and 19 have been cancelled in this Amendment, rendering the objection to the claims moot.

Rejections Under 35 U.S.C. § 102

In items 5 and 6 on pages 7 and 8 of the Office Action, the Examiner rejected claims 13 and 17 under 35 U.S.C. § 102(b) as being anticipated by Biggs et al. (U.S. Patent No. 5,410,669). Applicant respectfully traverses these rejections for the reasons presented below.

Claim 13 of the present invention recites, as amended, a "method of controlling a cache memory that is connected to a main memory with a first address space and capable of acting as a random access memory, ... comprising: ... assigning a second address space, which is **separate from the first address space** of the main memory, for the cache memory when the cache memory is acting as the random access memory" (emphasis added).

Biggs discloses that an instruction cache/SRAM module 14 operates in a cache mode or in a SRAM mode (Biggs at col. 4, line 46 to col. 5, line 25). However, Biggs does not disclose

"controlling a cache memory that is connected to a main memory with a first address space and capable of acting as a random access memory" in accessing the main memory through the cache memory, "determining whether the cache memory is acting as the random access memory; and assigning a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory" as recited in claim 13 of the present invention.

In the present invention, the address space when the cache memory is used and the address space when the main memory is used are separate from each other. Thus, various processes and circuits are not required to maintain coherence between the main memory and the random access memory, resulting in a high-speed, low-cost processor.

Claim 17 has been amended to depend from allowed independent claim 15.

Therefore, Applicants submit that claims 13 and 17 patentably distinguish over the prior art. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejections under § 102.

Rejections Under 35 U.S.C. § 103(a)

In items 3 and 4 on pages 2-7 of the Office Action, the Examiner rejected claims 1-12, 18, and 19 under 35 U.S.C. § 103(a) as being unpatentable over MacDonald (U.S. Patent No. 5,913,224) in view of Ekner et al. (U.S. Patent No. 6,092,159). Applicants have cancelled claims 1-12, 18, and 19 in this Amendment, rendering the § 103 rejection moot.

New Claims

Claims 21 and 22 are newly added with this response to alternatively define the present invention. Claim 21 has been added to reinstate originally filed claim 14. Claim 21 depends from independent claim 13 discussed above and is patentable over the prior art for at least the reasons discussed above.

Claim 22 has been added to reinstate claim 15 as originally filed. Similar to claim 13, claim 22 recites a "computer including a main memory and a cache memory, the main memory

having a first address space and the cache memory being capable of acting as a random access memory, comprising: a determination unit which determines whether the cache memory is acting as the random access memory; and an assignment unit which assigns a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory." These features are not taught or suggested by the cited references. Thus, for at least the reasons presented above, Applicants submit claim 22 patentably distinguishes over the prior art.

Accordingly, Applicants respectfully request allowance of the new claims.

Request for Return of Form PTO-1449

Applicants filed an Information Disclosure Statement with a Form PTO-1449 on September 28, 2000 and on August 27, 2001. Copies of these forms have not yet been returned to the applicant to confirm that the references cited therein have been considered. Accordingly, it is requested that the Examiner confirm consideration of these references by initialing and returning the 1449 forms. For convenience, copies of the 1449 forms are attached to this request.

CONCLUSION

It is submitted that none of the references, either taken alone or in combination, teach the present claimed invention. Thus, claims 13, 15, 17, and 20-22 are deemed to be in a condition suitable for allowance. Reconsideration of the claims and an early Notice of Allowance are earnestly solicited.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

Finally, if there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 5/29/03

By: C. Joan Gilsdorf
Christine Joan Gilsdorf
Registration No. 43,635

700 Eleventh Street, NW, Suite 500
Washington, D.C. 20001
(202) 434-1500

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please **AMEND** the following claims:

13. (TWICE AMENDED) A method of controlling a cache memory that is connected to a main memory with a first address space and capable of acting as a random access memory, which is executed by a computer that accesses the main memory through the cache memory, comprising:

determining whether the cache memory is acting as the random access memory; and

assigning a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory[,

wherein the computer includes a bus control unit connecting the main memory and the cache memory, and a peripheral system connected to the computer through the bus control unit, and

wherein, when the cache memory is acting as the random access memory and an access request externally sent from an address outside the second address space of the cache memory is received, the computer accesses one of the main memory or the peripheral system instead of the cache memory].

17. (TWICE AMENDED) [A] The computer [including a main memory and a cache memory, the main memory having a first address space and the cache memory being capable of acting as a random access memory,] according to claim 15, further comprising:

[a determination unit which determines whether the cache memory is acting as the random access memory;

an assignment unit which assigns a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory;]

a bus control unit connecting the main memory and the cache memory;

a peripheral system connected to the computer through the bus control unit; and

an access control unit which accesses one of the main memory or the peripheral system instead of the cache memory when the cache memory is acting as the random access memory

and an access request externally sent from an address outside the second address space of the cache memory is received.

Please **ADD** the following new claims:

21. (NEW) The method according to claim 13, wherein the computer includes a bus control unit connecting the main memory and the cache memory, and a peripheral system connected to the computer through the bus control unit, and wherein, when the cache memory is acting as the random access memory and an access request externally sent from an address outside the second address space of the cache memory is received, the computer accesses one of the main memory or the peripheral system instead of the cache memory.

22. (NEW) A computer including a main memory and a cache memory, the main memory having a first address space and the cache memory being capable of acting as a random access memory, comprising:

a determination unit which determines whether the cache memory is acting as the random access memory; and

an assignment unit which assigns a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory.